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This is a U.S. Patent Application for:

Title: THERMAL DISSIPATION IN INTEGRATED CIRCUIT SYSTEMS

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THERMAL DISSIPATION IN INTEGRATED CIRCUIT SYSTEMS

BACKGROUND

Integrated circuits typically are formed from semiconductor chips or dice supporting respective electronic circuits. Integrated circuits typically are packaged in hermetically sealed or plastic molded packages to prevent environmental degradation that otherwise might be caused by, for example, humidity, contaminants, and electrically charged species. In addition, current trends in integrated circuit design are increasing device functionality and shrinking device size. These trends are leading to an increase in the power dissipation requirements of semiconductor dice. For this reason, integrated circuits typically are packaged on carrier structures (e.g., flexible polyimide carriers, glass reinforced epoxy carriers, and ceramic circuit carriers) that include heat dissipation features for cooling the integrated circuit dice mounted within the packages.

In one common power dissipation approach, an integrated circuit package includes a metal heat sink that is bonded or laminated to a circuit carrier. In some approaches, the bottom (or back) side of the integrated circuit die (i.e., the side that is free of any electrical signal connections) is attached to the metal heat sink with an epoxy-based adhesive, which may contain thermally conductive particles that increase the thermal conductivity between the integrated circuit chip and the heat sink. In other approaches, the bottom side of the integrated circuit die is attached to the circuit carrier surface at locations that are electrically and thermally connected to one or more heat spreading elements. In one integrated circuit system of this type, the heat spreading elements are thermal solder balls, which are attached to the bottom of the package. This system also includes a silicone-based layer that is screened onto the top face of a semiconductor die during packaging to increase thermal conduction between the electronic component and an overlying heat spreader.

SUMMARY

In one aspect, the invention features an integrated circuit system that includes a die incorporating an integrated circuit. The die has a top side and a

bottom side. The top side supports an electrical signal communication metallization and a top side thermal dissipation metallization. The bottom side supports a bottom side thermal dissipation metallization.

In another aspect, the invention features a method of making an integrated circuit system. In accordance with this inventive method, multiple die regions each having an electrical signal communication metallization and a top side thermal dissipation metallization are formed on a top side of a substrate. A bottom side thermal dissipation metallization is formed on a bottom side of the substrate for each die region. The die regions are singulated to form respective integrated circuit dice.

Other features and advantages of the invention will become apparent from the following description, including the drawings and the claims.

DESCRIPTION OF DRAWINGS

FIG. 1A is a diagrammatic top view of an embodiment of an integrated circuit die.

FIG. 1B is a diagrammatic cross-sectional side view of the integrated circuit die embodiment of FIG. 1A taken along the line 1B-1B.

FIG. 2 is a diagrammatic cross-sectional side view of the integrated circuit die embodiment of FIG. 1A incorporated within an embodiment of an integrated circuit package.

FIG. 3 is a flow diagram of an embodiment of a method of manufacturing the integrated circuit die embodiment of FIG. 1A.

FIGS. 4A and 4B are diagrammatic top and side views of a substrate containing a plurality of die regions corresponding to the integrated circuit die embodiment of FIG. 1A.

FIG. 5A is a diagrammatic top view of an embodiment of an integrated circuit die.

FIG. 5B is a diagrammatic cross-sectional side view of the integrated circuit die embodiment of FIG. 5A taken along the line 5B-5B.

FIGS. 6 and 7 are diagrammatic top views of alternative top side thermal dissipation metallizations for different respective embodiments of integrated circuit dice.

DETAILED DESCRIPTION

In the following description, like reference numbers are used to identify like elements. Furthermore, the drawings are intended to illustrate major features of exemplary embodiments in a diagrammatic manner. The drawings are not intended to depict every feature of actual embodiments nor relative dimensions of the depicted elements, and are not drawn to scale.

The embodiments described in detail below feature integrated circuit systems with thermal dissipation enhancement features that allow direct metallurgical bonds to be formed between the top and bottom sides of integrated circuit dice and heat spreading elements of an integrated circuit package. These metallurgical bonds simultaneously provide high thermal conductivity paths for heat emanating from the integrated circuit dice and robust attachments to the integrated circuit packages. In this way, these embodiments provide an effective way to remove heat from the integrated circuit dice and maintain the temperature of the integrated circuit dice within a reliable temperature range, while increasing the mechanical stability of the integrated circuit dice and increasing the overall robustness of the integrated circuit packages. In addition, these thermal dissipation enhancement features may be formed using substrate-scale (e.g., wafer-scale) processing, thereby increasing processing efficiency and allowing the integrated circuit dice to be packaged using standard automatic metallurgical bonding equipment.

FIGS. 1A and 1B show an embodiment of a die 10 that incorporates an integrated circuit 12. The term "die" refers to a substrate (usually part of a larger substrate) that contains an integrated circuit. The die 10 may be formed of any material that is suitable for supporting or containing integrated circuit 12. In some implementations, the die 10 is formed of a semiconductor material, such as silicon, gallium arsenide, or indium phosphide. As used herein, the term "integrated circuit" broadly refers to an electronic or optoelectronic component that is mountable on a substrate supporting one or more electrically conductive traces (or paths or channels), which are designed to carry electrical signals between the integrated circuit and one or more other electronic or optoelectronic components.

The die 10 has a top side 14 that supports an electrical signal communication metallization 18 and a top side thermal dissipation metallization 20. As used herein, the term "metallization" refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit. In the embodiment illustrated in FIGS. 1A and 1B, the electrical signal communication metallization 18 includes a set of bonding elements defining the electrical contact areas on the die 10 for electrical wires, lines or traces carrying electrical signals (e.g., input/output signals) between the integrated circuit 12 and one or more external components or devices. The top side thermal dissipation metallization 20 defines a thermal contact area on the top side 14 of die 10 that provides a high thermal conductivity path from the die 10 to, for example, a heat spreader of a package into which die 10 will be mounted. The electrical signal communication metallization 18 and the top side thermal dissipation metallization 20 may be formed of the same or different materials. In some implementations, the electrical signal communication metallization 18 is formed of one of the following materials: gold, gold alloy, aluminum, and aluminum alloy. In one implementation, the top side thermal dissipation metallization 20 is formed of copper.

The die 10 also has a bottom side 16 that supports a bottom side thermal metallization 17. The bottom side thermal metallization 17 defines a thermal contact area on the bottom side 16 of the die 10 that provides a high thermal conductivity path from the die 10 to, for example, a heat spreader of a package into which die 10 will be mounted. In one implementation, the bottom side thermal dissipation metallization 17 is formed of copper.

As shown in FIG. 1A, in the illustrated embodiment, the bonding elements of the electrical signal communication metallization 18 are disposed on the top side 14 of die 10 in a peripheral region 22 located between the two square virtual boundaries 24, 26. This arrangement of the electrical signal communication metallization 18 conforms to standard layout specifications for typical wirebonded integrated circuit dies, allowing die 10 to be incorporated readily into existing integrated circuit fabrication processes. The top side thermal dissipation metallization 20 is disposed on the top side of die 10 within a central region 28 surrounded by the peripheral region 22.

FIG. 2 shows an embodiment of an exemplary package 30 into which die 10 may be mounted. The package 30 includes a carrier substrate 32, a lid 34, and an electrical interface 36. The carrier substrate 32 may be any type of single- or multilayer substrate, including a printed circuit board (or printed wiring board) substrate, a glass substrate, and a ceramic substrate. The carrier substrate 32 includes a plurality of electrical wires, traces or channels leading from the electrical interface 36 to contact pads 38 on a die mounting surface 40. In the embodiment illustrated in FIG. 2, bond wires 42 connect the bonding elements of the electrical signal communication metallization 18 to respective contact pads 38 on the die mounting surface 40. The lid 34 may be mounted to the carrier substrate 32 using any type of suitable attachment method (e.g., an epoxy-based adhesive or a metallurgical bond, such as a solder bond).

The bottom side thermal dissipation metallization 17 may be metallurgically bonded directly to the carrier substrate 32, which then functions as a heat spreader. Alternatively, the bottom side thermal dissipation metallization 17 may be metallurgically bonded to a dedicated heat spreader 44, which is attached to the carrier substrate 32, as shown in FIG. 2. As used herein, the term "heat spreader" refers to any active or passive device or element designed to diffuse or dissipate heat. In one implementation, heat spreader 44 consists of a metal heat sink plate that is attached to the carrier substrate 32. The bottom side thermal dissipation metallization 17 is bonded metallurgically to the heat spreader 44 by a solder bonding process, such as surface mount technology (SMT) process. In alternative embodiments, bottom side thermal dissipation metallization 17 may be mounted to the carrier substrate using another mounting technique, such as, a bore soldering ("pin through-hole") mounting technique or a flip-chip mounting technique with an optional thermal compound backfill.

In the illustrated embodiment, the top side thermal dissipation metallization 20 is metallurgically bonded to the lid 34, which functions as a heat spreader. In this embodiment, the lid 34 is formed of a heat dissipation material, such as a metal (e.g., copper). In other embodiments, the top side thermal dissipation metallization 20 may be metallurgically bonded to a dedicated heat spreader that is attached to or incorporated within the lid 34.

In some embodiments, the enclosed space 48 between the lid 34 and the mounting surface 40 of the carrier substrate 32 is filled with an encapsulating material (e.g., an epoxy-based or a resin-based molding compound).

The metallurgical bonds between the top and bottom side thermal dissipation metallizations and the lid 34 and the heat spreader 44 simultaneously provide high thermal conductivity paths for heat emanating from the integrated circuit die 10 and robust attachments to the integrated circuit package. In this way, these bonds provide an effective way to remove heat from the integrated circuit die 10 and maintain the temperature of the integrated circuit die 10 within a reliable temperature range, while increasing the mechanical stability of the integrated circuit die 10 and increasing the overall robustness of the integrated circuit package 30.

In the embodiment illustrated in FIG. 2, the electrical interface 36 of package 30 includes a ball grid array, which includes an array of solder balls 46 that may be attached to corresponding contact pads on a component substrate (e.g., a printed circuit board) using, for example, SMT. In other embodiments, the electrical interface 36 may include different electrical elements that are compatible with a different package mounting technique, such as bore soldering ("pin through-hole") mounting technique or solder column bonding technique.

In some embodiments, one or more electrical contacts 49 of the integrated circuit embedded in die 10 may be connected electrically to one or more solder balls 46 by one or more electrical paths 51. Each electrical path 51 extends from the electrical contact 49, through the top side thermal dissipation metallization 20, through the metallurgical bond between the top side thermal dissipation metallization 20 and the lid 34, through the lid 34, through the bond between the lid 34 and the substrate 32, and through the substrate 32, to a solder ball 46. In some implementations of these embodiments, the electrical path 51 may be connected electrically to a source of power or ground potential.

Referring to FIGS. 3, 4A and 4B, in one embodiment, die 10 is manufactured as follows. In accordance with this inventive method, multiple die regions 10 are formed on a top side of a substrate 50 (e.g., a semiconductor wafer) (block 52). The die regions 10 that are formed on substrate 50 are separated from one another by street areas 54. Each die region 10 has an

electrical signal communication metallization 18 and a top side thermal dissipation metallization 20, as described in detail above. A bottom side thermal dissipation metallization 17 is formed on a bottom side of the substrate 50 for each die region (block 56). The bottom side thermal dissipation metallization 17 may be formed as a uniform layer or layers of metal that are deposited onto the bottom side of the substrate 50, as shown in FIG. 4B. Alternatively, the bottom side thermal dissipation metallization 17 may be patterned using, for example, photolithographic processing techniques. The die regions 10 are singulated to form respective integrated circuit dice (block 58).

Other embodiments are within the scope of the claims.

For example, in the embodiments described in detail above, the top side thermal dissipation metallization 20 consists of a single- or multi-layer film having a substantially uniform thickness. In other embodiments, the top side thermal dissipation metallization 20 may have a non-uniform thickness or it may be patterned. The top side thermal dissipation metallization pattern may be designed to reduce stress buildup in the integrated circuit die that might result from non-uniform heating effects or other causes.

FIGS. 5A and 5B show an embodiment of an integrated circuit die 60 that includes a top side thermal dissipation metallization 62 that has an array of through-holes 64, which help to reduce stress buildup in the integrated circuit die 60. Other embodiments may include different top side thermal dissipation metallization patterns. For example, FIG. 6 shows an embodiment of a top side thermal dissipation metallization 66 that is patterned in to a rectangular spiral shaped path. FIG. 7 shows an alternative embodiment of a top side thermal dissipation metallization 68 that is patterned into a rectangular zigzag path. Other embodiments may include non-rectangular-shaped top side thermal dissipation metallization patterns. These patterns may conform to regular shapes, such as circular shapes or polygonal shapes, or arbitrary shapes.

Still other embodiments are within the scope of the claims.